EMBEDDED SYSTEM
ENEX 302

Year/Part: III/I

Teaching Schedule				Examination Scheme						Total
				Theory			Practical			
L	T	P	Total	Assessment Marks	Final		Assessment Marks	Final		
					Duration (Hrs)	Marks		Duration (Hrs)	Marks	
3	1	1.5	5.5	40	3	60	25	0	0	125

Depth Codes

E-Explanation	C-Circuit	D-Definition	Dm-Demonstration
Dv-Derivation	Dw-Drawing	P-Proof	I-Illustration
Num-Numerical	Prg -Programming	S-State	CS - Case Study
MP- Mini Project	Exp -Experiment	Rev - Review / Recap	Cmp - Comparison

Unit	Topic/ Sub topic	Depth Code	Description of Depth	Actual plan			Week
				L	T	P	
1	**Introduction**			**2**			**1**
	1.1 Definition of embedded system	D,E	Define embedded system with relevant examples	0.25			
	1.2 Embedded system vs. general purpose computing system	E, Cmp	Comparison between general purpose computing system and embedded system	0.25			
	1.3 Characteristics, classification and purposes of embedded system	D,E	– **Characteristics**: Single functioned, tightly constrained, reactive & real time – **Classification** based on generation, complexity and performance requirements, deterministic behaviour, triggering – **Purpose** : Data collection / storage/ representation, data communication, signal processing, monitoring, control	1			
	1.4 Major application areas of embedded systems	D,E	Consumer electronics, household appliances, home automation and security systems, automotive industry, telecom, computer peripherals, networking systems, healthcare, measurement and instrumentation, banking and retail, etc.	0.5			

Unit	Topic/ Sub topic	Depth Code	Description of Depth	Actual plan			Week
				L	T	P	
2	**Core of Embedded System**			**6**			**1-3**
	2.1 Elements and core of embedded system	D,E,I	Elements of an embedded system (controller, sensors, actuators, memory, communication interface)	0.25			
	2.1.1 General purpose and domain specific processors: Microprocessor, microcontroller, digital	D,E,I,Cmp	– Brief introduction, examples and applications of microprocessor, microcontroller and digital signal processor – General purpose processor versus	0.25			

	signal processor (DSP)		Application specific instruction set processor				
	2.1.2 Application specific integrated circuits (ASICS)	D,E	Brief introduction, advantages, disadvantages and applications of ASICs	0.25			
	2.1.3 Programmable logic devices (PLDS)	D,E,I	Brief introduction, advantages, disadvantages and applications of PLDs	0.25			
	2.1.4 Commercial off-the-shelf components (COTS)	D,E,I	Brief introduction, advantages, disadvantages and applications of COTS	0.25			
	2.2 Sensors and actuators: LED, 7 segment display, optocoupler, stepper motor, relay, Piezo buzzer, push button switch, keyboard, PPI	D,E,I,C, Rev	– Definition of sensors and actuators – Brief discussion on working principle and applications of LED, 7 segment display, optocoupler, stepper motor, relay, piezo buzzer, push button switch, keyboard and PPI – Interfacing of stepper motor through driver circuit – Transistor based relay driving circuit	2			
	2.3 Communication interface: I2C, SPI bus, UART, 1 – wire interface, parallel interface, IEEE 1394 (Firewire), Wi-Fi, Zigbee, Bluetooth	D,E,I,C, Rev	Brief discussion on working principle and applications of I2C, SPI bus, UART, 1- wire interface, parallel interface, IEEE 1394 (Firewire), Wi-Fi, Zigbee, Bluetooth	1.5			
	2.4 Embedded firmware, real-time clock (RTC) and watchdog timer	D,E	– Definition of embedded firmware, methods available for developing the embedded firmware, HEX File Creation – Working and application of real time clock (RTC) and watchdog timer	0.75			
	2.5 Quality attributes of embedded systems						
	2.5.1 Operational quality attributes: Response, throughput, reliability, maintainability, security and safety	D,E	Definition and explanation of operational quality attributes : response, throughput, reliability, maintainability, security and safety	0.25			
	2.5.2 Non-operational quality attributes: Testability and debug-ability, evolvability, portability, time to prototype and market and per unit cost and NRE cost	D,E	Definition and explanation of non-operational quality attributes: testability and debug-ability, evolvability, portability, time to prototype and market and per unit cost and NRE cost	0.25			

Unit	Topic/ Sub topic	Depth Code	Description of Depth	Actual plan			Week
				L	T	P	
3	**Hardware Design Issues**			**6**	**4**		**3-5**
	3 . 1 Transistors and logic gates: Logic gates implementation using CMOS	D,E,C,I	Definition of transistors and logic gates, CMOS transistor implementation of some basic logic gates	**0.5**			
	3.2 Review of combinational logic	D,E,I	Basic Combinational Logic Design, RT-Level Combinational Components	**0.5**			
	3.3 Review of sequential logic	D,E,C,I	Flip flops, RT-Level Sequential Components, Sequential Logic Design	**1**			

	3.4 Design of custom single/dual purpose processor design	D,E,C,I	Design of custom single purpose processor Definition of dual purpose processor design	**2.5**	**3**		
	3.5 Optimization of custom single/dual purpose processor design	D,E,C,I	Optimizing the original program, Optimizing the FSMD, Optimizing the FSM Definition of optimization of dual purpose processor design	**1.5**	**1**		

Unit	Topic/ Sub topic	Depth Code	Description of Depth	Actual plan			Week
				L	T	P	
4	**Designing Embedded System with Microcontroller**			**10**	**5**		**5-8**
	4 . 1 Microprocessor versus microcontroller	Cmp	Compare microprocessor with microcontroller	**0.5**			
	4 . 2 Factors for selecting a microcontroller (Overview of 8051/AVR/PIC/ARM cortex microcontroller)	D,E,I	– General factors: Feature Set, Speed of Operation, Code and Data Memory Space, Development Support, Availability, Power consumption, Cost – A basic overview of 8051/AVR/PIC/ARM cortex microcontroller with factors to select them for different applications	**1**			
	4.3 Pin description of 8051	E,I	Pin diagram of 8051 microcontroller	**0.5**			
	4.4 Designing with 8051			**4**	**5**		
	4.4.1 8051 architecture	E,Dw,I	Block diagram representation of 8051 architecture				
	4.4.2 Memory organization: Program and data memory, external program and data memory interfacing	D,E,I,Dw	– Explanation with simplified block diagram of program memory organization – Explanation with simplified block diagram of 8051 external program and data memory chip interfacing				
	4.4.3 Registers	D,E,I	CPU registers and Scratchpad Registers				
	4.4.4 Interrupt and interrupt systems	D,E	Definition of Interrupt, use of interrupts, Interrupt System : enabling and disabling interrupt, setting interrupt priorities				
	4.5 Timer units	D,E,I	Timer/Counter in Mode 0, Mode 1, Mode 2 and Mode 3	**1**			
	4.6 Addressing modes and instruction set of 8051	D,E,I	– Addressing modes: Immediate, Register, Direct, register indirect, Indexed – All the relevant instruction set of 8051	**1**			
	4.7 Assembly programming	D,E	Assembly programming examples with 8051 (e.g. LED, switch, 7-segment, Delay, Pulse generation based on timer)	**2**			

Unit	Topic/ Sub topic	Depth Code	Description of Depth	Actual plan			Week
				L	T	P	
5	**Embedded System Development Environment**			**4**			**9,10**
	5 . 1 Integrated development environment (IDE)	D,E,I	Definition and explanation of IDE with various examples of IDEs for embedded firmware development	**0.5**			
	5 . 2 Keil µVision 3/4 IDE for 8051	E,I	Demonstrate the use of Keil µVision 3/4 IDE for 8051 microcontroller	**1.5**			

Unit	Topic/ Sub topic	Depth Code	Description of Depth	Actual plan			Week
				L	T	P	
	5.3 An overview of ides for embedded system development	E,I	Familiarity with some of the popular IDEs for some commonly used processors/controllers	**0.5**			
	5.4 Files generated on cross – compilation: List file (.lst), preprocessor output file, object file (.obj), map file (.map), hex file (.hex)	D,E,I	Explain and illustrate the contents of list file, preprocessor output file, object file, map file, hex file, Illustration of assembling process (from source code to executable file)	**1**			
	5.5 Simulators, emulators and debugging	D,E	– Definition, features, advantages and limitations of simulators – Definition and requirement of debugging, hardware and firmware debugging – Definition and requirement of emulators	**0.5**			

Unit	Topic/ Sub topic	Depth Code	Description of Depth	Actual plan			Week
				L	T	P	
6	**RTOS Based Embedded System Design**			**10**	**3**		**10-13**
	6.1 OS basics			**1**			
	6.1.1 Definition and primary functions	D,E,I	Basic components of an OS, Primary functions of an OS				
	6.1.2 Kernel and its services: Process management, primary and secondary storage management, file system management, I/O devices management, protection, interrupt handler	D,E,I	– Process management – Primary and secondary storage management File system management – I/O System (device) management – Protection Systems – Interrupt handler				
	6.1.3 Kernel space and user space: Monolithic and micro kernels	D,E,I	– Kernel space, User space – Monolithic Kernel Model, its pros and cons, examples – Microkernel Model, its pros and cons, examples				
	6 . 2 Types of OS: General purpose and real time OS	D,E	Characteristics of General Purpose OS (GPOS) and Real Time OS (RTOS), Examples of each	**0.5**			
	6.3 RT kernel and its basics functions			**1**			
	6.3.1 Task / process management	D,E	Brief definition and explanation on Task / process management				
	6.3.2 Task / process scheduling	D,E	Brief definition and explanation on Task / process scheduling				
	6.3.3 Task / process synchronization	D,E	Brief definition and explanation on Task / process synchronization				
	6.3.4 Error / exception handling	D,E	Brief definition and explanation on Error / exception handling				
	6.3.5 Memory management	D,E	Brief definition and explanation on Memory management				
	6.3.6 Interrupt handling	D,E	Brief definition and explanation on Interrupt handling				

	6.3.7 Time management	D,E	Brief definition and explanation on Time management				
	6.4 Hard real time and soft real time	D,E,Cmp	Definition of hard real time and soft real time system with examples, their comparison	**0.25**			
	6.5 Process: Structure of process, process state and transition and PCB	D,E	Memory organization of a process (stack, data, code memory), Generic representation of process states and state transition, Process management , Contents and functions of Process Control Block (PCB)				
	6.6 Threads			**1.5**			
	6.6.1 Concept of multithreading	D,E,I	Thread-process diagram, Advantages of multithreading				
	6.6.2 Thread standards: POSIX threads, Win32 threads, java threads	D,E,I	Introduction to thread standards, Thread creation and management				
	6.6.3 Thread preemption: User level thread, kernel/system level thread, many-to-one model, one-to-one model, many-to-many model	D,E	– Thread context switching, User level thread, Kernel/System level thread – Thread binding models : many-to-one model, one-to-one model, many-to-many model with their characteristics and examples.				
	6.6.4 Thread vs. process	Cmp	Basis of comparison : Unit of execution, memory, Resource allocation, Communication, Creation time, Context switching, Isolation, Crash Impact, Scheduling, etc.				
	6.7 Multiprocessing and multitasking: preemptive, non – preemptive and cooperative	D,E	Context switching, context saving, context retrieval Types of Multitasking : cooperative, preemptive, non-preemptive	**0.5**			
	6.8 Task scheduling	D,E,I		**4**	**3**		
	6.8.1 Factors for selecting a scheduling criterion	D	CPU Utilization, Throughput, Turnaround Time, Waiting Time, Response Time				
	6.8.2 Non-preemptive scheduling: FCFS/FIFO, LCFS/LIFO, SJF, priority based	D,E,Num	First-Come-First-Serve (FCFS)/ First-In-First-Out (FIFO) Scheduling, Last-Come-First-Served (LCFS) / Last-In-First-Out (LIFO) Scheduling, Shortest Job First (SJF) Scheduling, Priority Based Scheduling				
	6.8.3 Preemptive scheduling: SRTF, RR, priority based	D,E,Num	Preemptive Shortest Job First / Shortest Remaining Time (SRT) Scheduling, Round Robin (RR) Scheduling, Priority Based Scheduling				
	6.9 Deadlock			**1**			
	6.9.1 Conditions for deadlock	D,E	Mutual Exclusion, Hold and Wait, No Resource Preemption, Circular Wait				
	6.9.2 Deadlock handling: Ignore deadlocks, detect and recover, avoid deadlocks, prevent deadlocks, livelock and starvation	D,E	Ignore deadlocks, Detect and recover, Avoid deadlocks, Prevent deadlocks, Livelock, Starvation				
	6.10 How to choose an RTOS			**0.25**			
	6.10.1 Functional requirements	D,E	Processor Support, Memory Requirements, Real-time Capabilities, Kernel and Interrupt Latency, Inter-process Communication & Task Synchronisation, Modularisation				

			Support, Support for Networking and Communication, Development Language Support				
	6.10.2 Non – functional requirements	D,E	Custom Developed or Off the Shelf, Cost, Development & Debugging Tools Availability, Ease of Use, After Sales				

Unit	Topic/ Sub topic	Depth Code	Description of Depth	Actual plan			Week
				L	T	P	
7	**VHDL Coding and Logic Synthesis**			**4**	**3**		**13-14**
	7 . 1 Introduction, features, application, design flow and code structure	D,E,Dm	– Overview of VHDL: History and purpose – Features: Strong typing, concurrency, modularity – Applications: FPGA, ASIC design, digital system verification – VHDL Design Flow: Specification, Modeling, Simulation, Synthesis, Implementation – VHDL Code Structure: Library/Package declarations, Entity, Architecture	**0.5**			
	7 . 2 VHDL modeling styles: Behavioral model, dataflow model and structural model	D,E	Explanation of Behavioral, Dataflow and Structural model with their VHDL description	**0.5**			
	7.3 Lexical elements: Library and packages, identifiers, keywords, numbers, character, string, data objects, data types, operator, data type conversion	E,Dm	Library and packages, identifiers, keywords, numbers, character, string, data objects, data types, operator, data type conversion	**0.5**			
	7.4 Dataflow model: Concurrent statements	E,Dm	Simple concurrent signal assignments, Conditional signal assignments, Selected Signal assignments	**0.5**			
	7.5 Behavioral modeling: Sequential statements	E,Dm	Process, If statements, Case statements, The WAIT statement, The LOOP statement, Next and Exit statement, Null statement	**0.5**			
	7.6 Structural modeling	E,Dm	Component declaration, Component Instantiation and interconnections	**0.5**			
	7.7 Finite state machine (FSM) design using VHDL: Coding of counter, register, sequence detector and custom single/dual purpose processor	E, Prog, I, Dm	State transition diagram, FSM and its types: Mealy and Moore, VHDL template for FSMs, Mealy FSM, Moore FSM VHDL examples: counter, register, sequence detector and custom single/dual purpose processor	**1**	**3**		

Unit	Topic/ Sub topic	Depth Code	Description of Depth	Actual plan			Week
				L	T	P	
8	IC Technology			**3**			**15**
	8.1 Introduction	D,E,Dw	Introduction to IC Technology, IC manufacturing steps	**0.75**			
	8.2 Full-custom (VLSI) IC technology	D,E,I,Dw	Concept and application of VLSI with its advantages and disadvantages	**0.75**			
	8.3 Semi-custom (ASIC) IC technology	D,E,I,Dw	Concept and application of ASIC with its advantages and disadvantages	**0.75**			
	8.4 Programmable logic	D,E,I,Dw	Concept and application of PLD with its	**0.75**			

Unit	Topic/ Sub topic	Depth Code	Description of Depth	Actual plan			Week
				L	T	P	
	devices (PLD) IC technology		advantages and disadvantages				

References:

1.Shibu, K. V. (2012). Introduction to embedded systems. Tata McGraw Hill Education. (Unit 1,2,4,5 and 6)

2.Vahid, F., Givargis, T. (2011). Embedded system design: A unified hardware/software introduction. Wiley India. (Unit 1,3, and 8)

3.Lee, W. F. (2000). VHDL coding and logic synthesis with Synopsis. Academic Press. (Unit 7)

4.Neupane, M., Shrestha, S. (2020). Embedded system design principles and practice (1st ed.). Pratibha Pustak Sadan and Stationery. (Units as per relevance)

Model Question

Q. N.	Questions	Chapter / Unit	Marks
1.	Define embedded system with its relevant examples. Define simulators and mention features, advantages and limitations of simulators in brief.	1 & 5	[2+4]
2.	(a) Give a brief introductioin to ASICS with its advantages, disadvantages and applications. (b) Describe the significance of I^2C serial communication protocol.	2	[4] [4]
3.	Design a single-purpose processor that outputs Fibonacci numbers up to n places. Start with a function computing the desired result, translate it into a state diagram and sketch a probable datapath.	3	[8]
4.	(a) Explain the addressing modes used in 8051 microcontroller with example. (b) Write an assembly language program to blink 8 LEDs connected at Port 2 of the 8051 microcontroller.	4	[4] [8]
5.	(a) Explain the basic functions of Real-time kernel. Differentiate between Monolithic Kernel and Micro Kernel. (b) Three processes with process IDs P1, P2, P3 with estimated completion time 10, 5, 7 milliseconds respectively enters the ready queue together in the order P1, P2, P3. Calculate the waiting time and Turn Around Time (TAT) for each process and the average waiting time and Turn Around Time (Assuming there is no I/O waiting for the processes).	6	[2+4] [6]
6.	What is behavioral modeling? Write VHDL code for 2-input multiplexer.	7	[2+6]
7.	What is photolithography and what are its types? Describe briefly about Full custom VLSI technology	8	[6]

Note: *Number of questions and distribution of marks are indicative only.*