COMPUTER ORGANIZATION AND ARCHITECTURE
ENCT 303

Year/Part: III/I

Teaching Schedule				Examination Scheme						
				Theory			Practical			
L	T	P	Total	Assessment Marks	Final		Assessment Marks	Final		Total
					Duration (Hrs)	Marks		Duration (Hrs.)	Marks	
3	1	1.5	5.5	40	3	60	25	0	0	125

Depth Codes

E-Explanation	C-Circuit	D-Definition	DM-Demonstration
DV-Derivation	DW-Drawing	P-Proof	I-Illustration
NUM-Numerical	PRG-Programming	S-State	ACT-Activity-based Learning
MP- Mini Project	EXP-Experiment	REV-Review / Recap	PS- Problem Solving
QA- Question Answer	Q- Quiz	ST- Surprise Test	MT-Mid Term Test

Unit	Topic/ Sub topic	Depth Code	Description of Depth	Actual plan			Week
				L	T	P	
1	**Introduction**						
	1.1 Organization and Architecture	E, D	Introduction to computer organization and computer architecture with their significances and differences	0.5			**1**
	1.2 Structure of a computer, single processor, multi-core computer	E, I	Structure of a computer, single processor, multi-core computer	1			**1**
	1.3 Performance Assessment 1.3.1 Clock speed and instruction per second 1.3.2 Instruction execution rate: CPI, MIPS rate, MFLOPS rate, arithmetic mean, harmonic mean, speed metric, geometric mean, rate metric, Amdahl's law, speed up	NUM, PS	Instruction execution rate: CPI, MIPS, MFLOPS, arithmetic mean, harmonic mean, speed metric, geometric mean, rate metric, Amdahl's law, speed up formulas with numerical examples	1			**1**
	1.4 Computer function Instruction Fetch and Execute Instruction cycle state diagram	DW, I	State diagram of instruction fetch and execute cycle with and without interrupt cycle	1.5			**1**
	Numerical examples on performance assessment	NUM	Numerical examples		2		**2**
	1.5 Computer component, interconnection structure, bus interconnection, PCI	DW, E	Computer components with their interconnection structure, bus interconnections, types and PCI interface	0.5			**2**
	1.6 RISC architecture, Overlapped register window Berkeley RISC	E	RISC concepts, overlapped register window and Berkeley RISC explanation	1.5			**2**

Unit	Topic/ Sub topic	Depth Code	Description of Depth	Actual plan			Week
				L	T	P	
	Evaluation	QA, Q					

Unit	Topic/ Sub topic	Depth Code	Description of Depth	Actual plan			Week
				L	T	P	
2	**Central Processing Unit (CPU)**						
	2.1 Processor Bus Organization	E	CPU bus signals and flow, diagrams and explanation	1			**3**
	2.2 Processor register Organization: Control word, examples of microoperations	I, E	Processor register organization Control word and microoperations of Control Unit. Microoperations of various instructions	1			**3**
	2.3 Stack Organization Register stack, memory stack, reverse polish notation, evaluation of arithmetic expressions	NUM	Stack Organization Register stack, memory stack, reverse polish notation, evaluation of arithmetic expressions Usage of Register and memory stack	1			**3**
	2.4 Instruction formats: CPU organization, zero and more address instruction formats	E, NUM	Instruction formats: CPU organization, zero and more address instruction formats Evaluation of an expression in 0, 1, 2, 3 address instruction formats	1			**3**
	2.5 Addressing modes: Types, examples, strengths and weaknesses	E, I	Addressing modes: Types, examples, strengths and weaknesses	1			**4**
	2.6 Instruction set	E	Data transfer and data manipulation instructions: Arithmetic, logical and shift operations, program control instruction explanation and examples	1			**4**
	2.7 Status bit conditions	I	Status bit flags: Carry, overflow, sign, zero	0.5			**4**
	2.8 Interrupt: Definition, types, processing and ISR	E	Types of Interrupts and ISR flow diagram	0.5			**4**
		NUM	Coding examples of different instruction formats		2		**4,5**
	Evaluation	QA, Q					

Unit	Topic/ Sub topic	Depth Code	Description of Depth	Actual plan			Week
				L	T	P	
3	**Control Unit (CU)**						
	3.1 Hardwired control unit	E	Hardwired control unit diagram and explanation	1			**5**
	3.2 Microprogrammed control unit	E, I	Microprogrammed control unit diagram and explanation	1			**5**
	3.3 Microinstructions, control memory organization, Wilkes control	DW	Micro instruction format, control memory, Wilkes control architecture: diagram and explanation	1			**5**
	3.4 Microinstruction sequencing: Design considerations, sequencing techniques, address generation, microinstruction encoding	E	Microinstruction sequencing: Design considerations, sequencing techniques, address generation, microinstruction encoding Next address generation using micro instruction sequencing	1			**6**
	3.5 Application of microprogramming	E	Application of microprogramming	0.5			**6**
	3.6 Microinstruction execution	E	Process of microinstruction execution	0.5			**6**
		NUM	Microprogramming examples in CU		2		**6**
	Evaluation	QA, Q					

Unit	Topic/ Sub topic	Depth Code	Description of Depth	Actual plan			Week
				L	T	P	
4	**Memory System**						
	4.1 Characteristics of memory system	D, E	Characteristics of memory system: Access time, cycle time, bandwidth explanation	1			**7**
	4.2 Memory classification and hierarchy	E, DW	Memory classification and hierarchy: Register, Cache memory, Main memory, Virtual memory	1			**7**
	4.3 Semiconductor memory and its types, read only memory, read/write memory	E, I	Semiconductor memory and its types: RAM (SRAM and DRAM), ROM (ROM, PROM, EPROM, EEPROM), Flash memory	1			**7**
	4.4 RAM modules and interfaces: DDR, DIMM and SODIMM	I, E	RAM modules and interfaces: DDR, DIMM, SODIMM explanation	1			**7**
	4.5 Cache memory	E, NUM, DW	Cache principles explanation, Elements of cache design: Cache size, mapping function, replacement algorithms, write policy, block size, single and multilevel caches and unified versus split cache, mapping, replacement, write policy	2			**8**
	4.6 External Memory	E	Magnetic Disk, RAID level 1 to 5, optical memory, Magnetic tape, SSD	1			**8**

Unit	Topic/ Sub topic	Depth Code	Description of Depth	Actual plan			Week
				L	T	P	
		NUM	Numerical on cache memory mapping: Hit and miss ratio		2		**8,9**
	Evaluation	QA, Q					

Unit	Topic/ Sub topic	Depth Code	Description of Depth	Actual plan			Week
				L	T	P	
5	**Computer Arithmetic**						
	5.1 ALU (Arithmetic and logic unit)	D, E	ALU components and operation, design steps	1			**9**
	5.2 Integer representation: Sign-magnitude representation, two's complement representation, converting between different bit lengths, fixed-point representation	E, DW	Integer representation: Sign-magnitude representation, two's complement representation, converting between different bit lengths, fixed-point representation	1			**9**
	5.3 Integer arithmetic	E, I	Addition, subtraction, multiplication (Unsigned, signed using Booth) and division algorithm (Restoring and non-restoring) Flowchart with examples	3			**9,10**
	5.4 Floating-point arithmetic	I, E	Floating-point representation: Principles, IEEE standard for binary floating-point arithmetic algorithm, addition, subtraction, multiplication and division algorithm	2			**10**
		NUM	Numerical examples on design of arithmetic circuit, logic circuit and ALU for various arithmetic algorithms		2		**11**
	Evaluation	QA, Q					

Unit	Topic/ Sub topic	Depth Code	Description of Depth	Actual plan			Week
				L	T	P	
6	**Pipelining and Vector Processing**						
	6.1 Pipelining and its importance	E	Different stages of Pipelining and their significances	0.5			**12**
	6.2 Instruction and arithmetic pipelining	E	Instruction and arithmetic pipelining	0.5			**12**
	6.3 Pipelining hazards: Data, structural and control hazards	PS	Pipelining hazards: Data, structural and control hazards	1			**12**
	6.4 RISC pipeline	I	RISC execution stages	0.5			**12**

Unit	Topic/ Sub topic	Depth Code	Description of Depth	Actual plan			Week
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	6.5 Parallel processing	E	Parallel Processing types	0.5			**12**
	6.6 Vector processing	E	Vector operations, Matrix multiplication, Memory interleaving, Superscalar processors, Supercomputers explanation	0.5			**13**
	6.7 Array processors: Attached array processor and SIMD array processor	E	Array processors: Attached array processor and SIMD array processor	0.5			**13**
	Evaluation	QA, Q					

Unit	Topic/ Sub topic	Depth Code	Description of Depth	Actual plan			Week
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7	**Input/ Output**						
	7.1 External devices	E	External device characteristics	0.5			**13**
	7.2 I/O modules: Module function, module structure	E	I/O modules: Block diagram of I/O modules with functions	0.5	0.5		**13**
	7.3 Programmed I/O, I/O commands, I/O instructions, flowchart	PS	Programmed I/O, I/O commands, I/O instructions Flowcharts with explanation	0.5	0.5		**13**
	7.4 Interrupt driven I/O, interrupt processing and flowchart	I	Interrupt driven I/O, interrupt processing ISR, flowcharts	0.5	0.5		**13**
	7.5 Direct memory access (DMA): Drawbacks of programmed and interrupt driven I/O, DMA function, typical DMA block diagram and possible DMA configuration	E	Direct memory access (DMA): Drawbacks of programmed and interrupt driven I/O, DMA function, typical DMA block diagram and possible DMA configuration Comparison and working principles	1	0.5		**13,14**
	7.6 I/O channels and processors: The evolution of the I/O function, characteristics of I/O channels	E	I/O channels and processors: The evolution of the I/O function, characteristics of I/O channels, features of I/O channels	1			**14**
	7.7 The external interface: Types of interfaces, point-to point and multiple configurations, small computer system interface (SCSI)	E	The external interface: Types of interfaces, point-to point and multiple configurations, small computer system interface (SCSI)	1			**14**
	Evaluation	QA, Q					

Unit	Topic/ Sub topic	Depth Code	Description of Depth	Actual plan			Week
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8	**Multiprocessor System**						
	8.1 Multiprocessor computers and their characteristics	E	Multiprocessor computers and their characteristics	1			**15**
	8.2 Multi-core computers and their architecture	E, I	Multi-core computers and their architecture	0.5			**15**
	8.3 Interconnection structure: Time-shared common bus, multiport memory, crossbar switch, multistage switching network and hypercube system	E, DW	Explanation of types of interconnection structures Time-shared common bus, multiport memory, crossbar switch, multistage switching network and hypercube system Comparison between them	1.5			**15**
	8.4 Interprocessor arbitration	E	Explanation of interprocessor arbitration	1			**15**
	8.5 Interprocessor communication and Synchronization	E, DW	Interprocessor communication explanation with synchronizing process	1			**15**
	Evaluation	QA, Q					

References: (Primarily based on the syllabus, and relevant chapters may be consulted as needed)

1. Stallings, W. (2018). Computer organization and architecture. Prentice Hall of India.
2. Mano, M. M. (2008). Computer system architecture. Pearson Education.
3. Hennessy, J. L., Patterson, D. A. (2000). Computer architecture: A quantitative approach. Harcourt Asia.

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QN	Question	Marks	Unit
1	Differentiate between Computer organization and architecture. Draw the instruction cycle state diagram with interrupt.	(3+3)	1
2	Write a code for X=((A+B) *(C-D)) /E using three address, two address, one address and zero address format.	6	2
3	What do you mean by addressing modes? List out its types and explain them with examples.	4	2
4	Differentiate between Hardwired and Microprogrammed Control Unit. Explain with diagram the working of microprogram sequencer for control memory.	(2+4)	3
5	Explain the characteristics of a memory system briefly. Explain direct cache mapping technique with example.	5	4
6	Explain different write policy techniques in cache memory.	5	4
7	Explain Booth's algorithm. Multiply -9 X -5 using Booth's multiplication algorithm.	6	5
8	Explain floating point division algorithm with example.	4	5
9	Explain six stage instruction pipelines with examples. Draw a time space diagram for 5 segments and 7 tasks.	6	6
10	Why IOP is used in input-output organization? With the help of a neat diagram, explain how DMA technique is used to transfer data in a computer system.	(2+4)	7
11	Compare and contrast different interconnection structures.	6	8

Note: *Number of questions and distribution of marks are indicative only.*