COMPUTER ORGANIZATION AND ARCHITECTURE

ENEX 253

Lecture : 3 **Year : II**
Tutorial : 1 **Part : II**
Practical : 3/2

Course Objectives:
The objective of this course is to provide the organization, architecture and designing concept of computer system including processor architecture, computer arithmetic, memory system, I/O organization and multicore.

1 Introduction (6 hours)

1.1 Organization and architecture
1.2 Structure and function
1.3 The evolution of computer architecture (RISC, CISC, BERKELEY RISC I, overlapped register window)
1.4 Performance assessment
  1.4.1 Clock speed and instruction per second
  1.4.2 Instruction execution rate: CPI, MIPS Rate, MFLOPS rate, arithmetic mean, harmonic mean, speed metric, geometric mean, rate metric, Amdahl's law, speed up
1.5 Computer function
  1.5.1 Instruction fetch and execute
  1.5.2 Instruction cycle state diagram
1.6 Interconnection structure, bus interconnection, multilevel bus hierarchy, PCI

2 Central Processor Organization (6 hours)

2.1 Processor bus organization
2.2 ALU: Arithmetic circuit, logic circuit, one and multi-stage ALU, shifter
2.3 Instruction formats: CPU organization, zero and more address instruction formats
2.4 Addressing modes
2.5 Instruction set
  2.5.1 Data transfer instruction
  2.5.2 Data manipulation instruction: Arithmetic, logical and shift operations
  2.5.3 Program control instruction
2.6 Status bit conditions

3 Control Unit (5 hours)

- 3.1 Definition, block diagram, control signals
- 3.2 Hardwired and microprogrammed CU
- 3.3 Microprogramming approach
  - 3.3.1 Control memory and its organization
  - 3.3.2 Computer organization
  - 3.3.3 Microprogram organization
  - 3.3.4 Address sequencing
  - 3.3.5 Mapping of microoperations
  - 3.3.6 Microinstruction formats
  - 3.3.7 Microprogramming examples
  - 3.3.8 Microprogram sequencer
  - 3.3.9 Field decoding

4 Memory System (8 hours)

- 4.1 Characteristics of memory system
- 4.2 Memory classification and hierarchy
- 4.3 RAM (SRAM and DRAM) and ROM organization: Circuit level implementation
- 4.4 Locality of reference
- 4.5 Cache memory principle
  - 4.5.1 Cache and main memory
  - 4.5.2 Cache / main memory structure
  - 4.5.3 Cache read operation
  - 4.5.4 Typical cache organization
  - 4.5.5 Elements of cache design (Cache address, cache size, mapping techniques, replacement algorithms, write policy, line size, number of caches)

5 Computer Arithmetic (8 hours)

- 5.1 Integer and floating-point representation
- 5.2 Integer arithmetic
  - 5.2.1 Addition and subtraction
  - 5.2.2 Multiplication
  - 5.2.3 Division
- 5.3 Floating-point arithmetic
  - 5.3.1 Addition and subtraction
  - 5.3.2 Multiplication
  - 5.3.3 Division

6 Pipelining and Vector Processing (4 hours)

6.1 Pipelining concept
6.2 Types of pipelining: Instruction and arithmetic pipelining
6.3 The major hurdle and hazards of pipelining: Data, structure and control hazards
6.4 Vector computation
  6.4.1 Vector computation approach
  6.4.2 Implementation: Pipelined ALU, parallel ALU and parallel processors

7 Input Output (I/O) Organization (4 hours)

7.1 Peripheral device
7.2 I/O modules
7.3 I/O interface
7.4 Modes of transfer
  7.4.1 Programmed I/O
  7.4.2 Interrupt driven I/O
  7.4.3 DMA
7.5 I/O processor
7.6 Data communication processor

8 Multicore Computer (4 hours)

8.1 Multicore computer
8.2 Hardware performance issues
  8.2.1 Increase in parallelism
  8.2.2 Power consumption
8.3 Software performance issue: Software in multicore
8.4 Multicore organization

Tutorial (15 hours)

1. Numerical examples on performance assessment
2. Design of arithmetic circuit, logic circuit and ALU
3. Coding examples covering different instruction formats
4. Microprogramming examples in CU
5. Cache memory mapping: Hit and miss ratio
6. Numerical examples for various arithmetic algorithms

Practical (22.5 hours)

1. Programming / simulation for addition and subtraction algorithm
2. Programming / simulation for multiplication algorithm
3. Programming / simulation for division algorithm
4. Programming / simulation for cache mapping techniques
5. Programming / simulation for ALU
6. Programming / simulation for vector processing

Final Exam

The questions will cover all the chapters in the syllabus. The evaluation scheme will be as indicated in the table below:

Chapter	Hours	Marks distribution*
1	6	8
2	6	8
3	5	8
4	8	10
5	8	10
6	4	5
7	4	5
8	4	6
Total	**45**	**60**

* There may be minor deviation in marks distribution.

References

1. Stalling, W. (2018). Computer Organization and Architecture. Pearson Education INC.
2. Mano, M. M. (2008). Computer System Architecture. Pearson Education INC.
3. Hennessy, J. L. Patterson D. A., (2000). Computer Architecture - A Quantitative Approach. Harcourt Asia PTE Ltd.